

# DATA SHEET

**SAA7280**

**Terrestrial Digital Sound Decoder  
(TDSD)**

Preliminary specification  
IC01

July 1991

**Philips Semiconductors**



**PHILIPS**

# Terrestrial Digital Sound Decoder (TDS)

# SAA7280

## FEATURES

- Full EBU NICAM 728 specification decoder
- Microcomputer controlled by I<sup>2</sup>C-bus
- Automatic decoding and output configuration depending upon transmission:
  - digital stereo
  - digital mono and data
  - 2 independent mono signals
- On board RAM for de-interleaving and 10 to 14 bit word expansion
- 7 sample interpolator for erroneous samples
- 3 times digital over-sampling filter (selectable)
- I<sup>2</sup>S sound bus output format
- I<sup>2</sup>C-bus transceiver enabling a master device to read:
  - status information
  - error count byte
  - additional data bits
 and write:
  - switch control codes
  - decoder control
- Status information and decoder control available via external pins.

## APPLICATIONS

- Television receivers
- Video cassette recorders

## GENERAL DESCRIPTION

Performing all digital decoding functions for a NICAM 728 digital stereo sound system, the SAA7280 is a CMOS integrated circuit which operates in conjunction with a DQPSK (Differential Quadrature Phase Shift Keying) demodulator (TDA8732) and a dual DAC (TDA1543). The device may also be

## QUICK REFERENCE DATA

| SYMBOL                       | PARAMETER                     | MIN. | TYP.   | MAX. | UNIT |
|------------------------------|-------------------------------|------|--------|------|------|
| V <sub>DD</sub>              | supply voltage range          | 4.5  | 5.0    | 5.5  | V    |
| I <sub>DD</sub>              | supply current                | -    | 50     | -    | mA   |
| f <sub>X<sup>T</sup>AL</sub> | crystal frequency             | -    | 17.472 | -    | MHz  |
| T <sub>amb</sub>             | operating ambient temperature | 0    | -      | 70   | °C   |

## ORDERING INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE |              |          |        |
|----------------------|---------|--------------|----------|--------|
|                      | PINS    | PIN POSITION | MATERIAL | CODE   |
| SAA7280P             | 28      | DIL          | plastic  | SOT117 |

## PIN CONFIGURATION

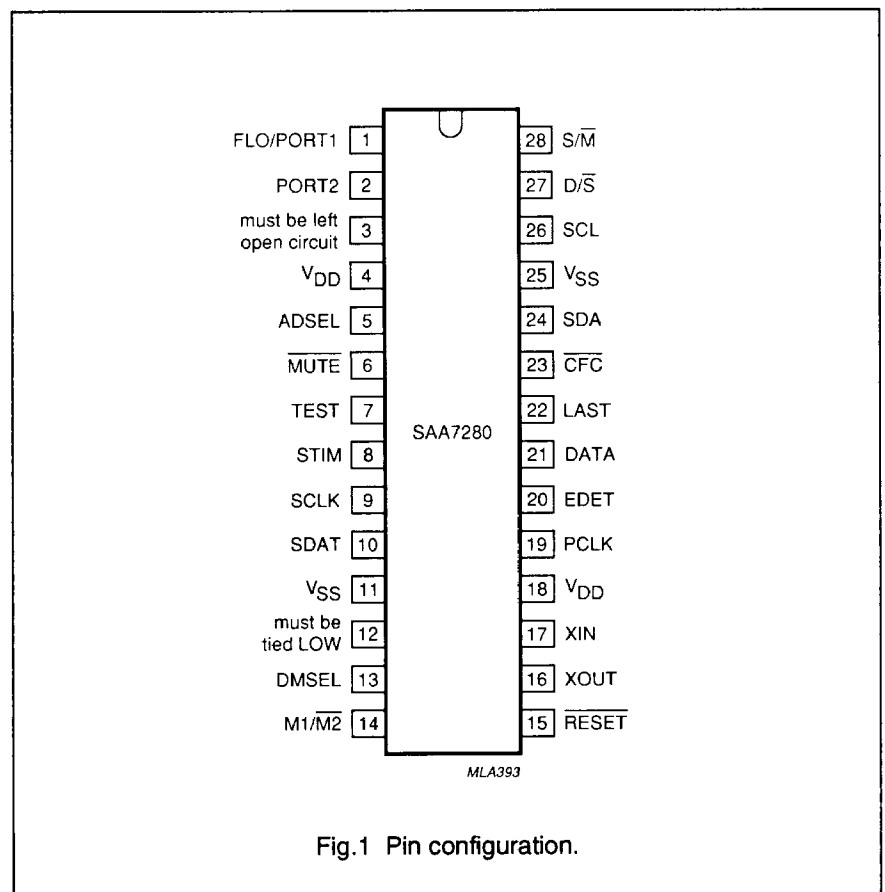


Fig.1 Pin configuration.

interfaced to other DQPSK demodulators and DACs.

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BLOCK DIAGRAM

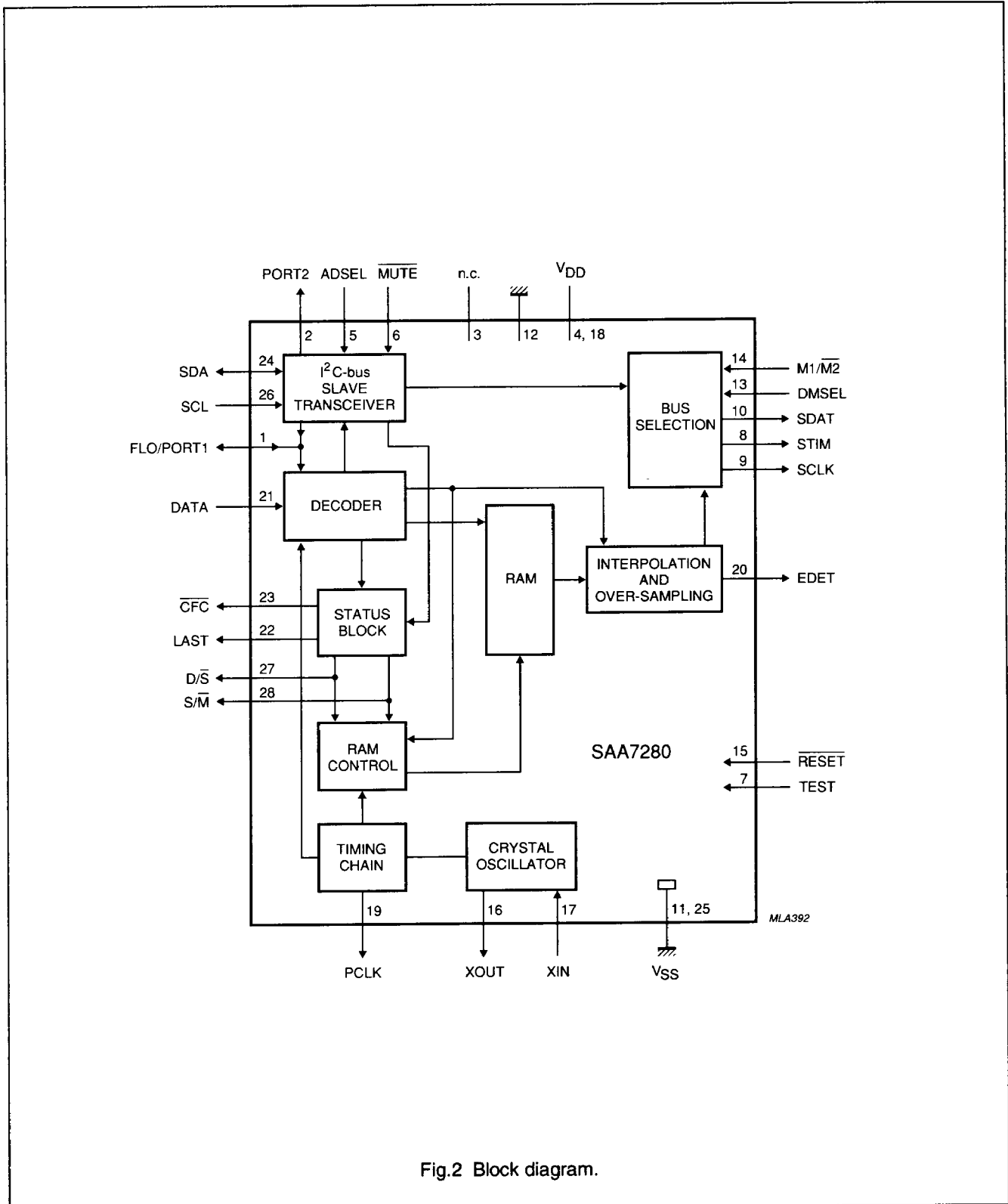


Fig.2 Block diagram.

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## PINNING

| SYMBOL          | PIN                | DESCRIPTION   |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
|-----------------|--------------------|---|-------|--------------------|----|----|----|-----|--|--|-----|--|----|----|----|----|----|----|----|--|------|---|---|---|---|---|---|---|---|-----|---|---|---|---|---|---|---|---|
| FLO/PORT1       | 1                  | I/O reserve sound switching flag override when selected as an input which is used in the logical equation for the 'LAST' output. Defaults to an input but can be set by control of the I <sup>2</sup> C-bus. Becomes a port output pin when selected by PT1EN bit in the I <sup>2</sup> C-bus of the control register with control via bit PORT1.   |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| PORT2           | 2                  | provides an output port controlled by bit PORT2 via the I <sup>2</sup> C-bus interface control register. (See Fig.3)  |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| n.c.            | 3                  | not used; must be left open-circuit.  |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| V <sub>DD</sub> | 4, 18              | +5 V power supply   |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| ADSEL           | 5                  | I <sup>2</sup> C-bus slave address selection input. Allows selection of one of two separate slave addresses.<br><table border="1" style="margin-left: 20px;"> <thead> <tr> <th>ADSEL</th> <th colspan="7">TDSD Slave Address</th> <th>R/W</th> </tr> <tr> <th></th> <th>A6</th> <th>A5</th> <th>A4</th> <th>A3</th> <th>A2</th> <th>A1</th> <th>A0</th> <th></th> </tr> </thead> <tbody> <tr> <td>HIGH</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>X</td> </tr> <tr> <td>LOW</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>X</td> </tr> </tbody> </table> | ADSEL | TDSD Slave Address |    |    |    |     |  |  | R/W |  | A6 | A5 | A4 | A3 | A2 | A1 | A0 |  | HIGH | 1 | 0 | 1 | 1 | 0 | 1 | 1 | X | LOW | 1 | 0 | 1 | 1 | 0 | 1 | 0 | X |
| ADSEL           | TDSD Slave Address |   |       |                    |    |    |    | R/W |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
|                 | A6                 | A5  | A4    | A3                 | A2 | A1 | A0 |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| HIGH            | 1                  | 0   | 1     | 1                  | 0  | 1  | 1  | X   |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| LOW             | 1                  | 0   | 1     | 1                  | 0  | 1  | 0  | X   |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| MUTE            | 6                  | when asserted will mute the SDAT output samples. Sets sample values to zero. Input is active LOW in non-I <sup>2</sup> C-bus applications. With I <sup>2</sup> C-bus active, mute polarity can be set by SC3 bit to 'exclusive-OR' operation (see Fig. 3).  |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| TEST            | 7                  | normally connected to V <sub>SS</sub> .   |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| STIM            | 8                  | sound bus output timing signal (I <sup>2</sup> S word selection).   |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| SCLK            | 9                  | sound bus output clock (I <sup>2</sup> S clock).  |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| SDAT            | 10                 | sound bus data output pin (I <sup>2</sup> S data).  |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| V <sub>SS</sub> | 11, 25             | ground (0 V).   |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| n.c.            | 12                 | not used. Must be tied LOW.   |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| DMSEL           | 13                 | active HIGH 'dual mono selection' input. Selects M1 and M2 as the output signals when the incoming transmission comprises two independent mono signals.   |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| M1/M2           | 14                 | 'M1' (M1/M2 = 1) or 'M2' (M1/M2 = 0) selection input when the input transmission consists of two independent mono signals (see Fig. 3).   |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| RESET           | 15                 | active LOW reset input to initialise device (e.g. at power-up).   |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| XOUT            | 16                 | respectively, the output and input of a single stage inverter used to provide a crystal oscillator maintaining circuit (with external biasing) or a simple CMOS input at XIN for the 17.472 MHz   |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| XIN             | 17                 | master clock  |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| PCLK            | 19                 | 728 kHz clock output derived from 17.472 MHz crystal.   |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| EDET            | 20                 | active HIGH error detection output.   |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |
| DATA            | 21                 | serial data at 728 Kbits/s from DQPSK demodulator.  |       |                    |    |    |    |     |  |  |     |  |    |    |    |    |    |    |    |  |      |   |   |   |   |   |   |   |   |     |   |   |   |   |   |   |   |   |

# Terrestrial Digital Sound Decoder (TDSD)

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| SYMBOL | PIN  | DESCRIPTION  |      |                                |     |      |  |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |
|--------|------|--|------|--------------------------------|-----|------|--|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|
| LAST   | 22   | <p>logic 'AND' status providing status of VDSP.(RSSF+FLO) (see Fig 3).</p> <p>VDSP, "valid digital sound present" signal. When HIGH this output indicates that the decoder is operating with a valid NICAM digital input which carries at least one sound channel. RSSF "or" FLO.</p> <p>FLO is a RSSF override signal which allows a user to turn off the RSSF input to the 'LAST' function. The purpose of this is to disable the RSSF input to the logical AND status pin (LAST) thus allowing the user to determine whether there is a reserve sound switching capability when the decoder is out of sync or receiving 'transparent data'.</p> <p>RSSF is a signal which indicates the reserve sound switching status. When HIGH this output shows that the conventional analogue FM signal is the same as the digital signal being decoded. Thus a failure of the digital signal can result in the circuit switching to conventional analogue sound.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>VDSP</th> <th>RSSF</th> <th>FLO</th> <th>LAST</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>X</td> <td>X</td> <td>0</td> <td rowspan="4">Where 'X' denotes "don't care"</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>X</td> <td>1</td> <td>1</td> </tr> </tbody> </table> | VDSP | RSSF                           | FLO | LAST |  | 0 | X | X | 0 | Where 'X' denotes "don't care" | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | X | 1 | 1 |
| VDSP   | RSSF | FLO  | LAST |                                |     |      |  |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |
| 0      | X    | X  | 0    | Where 'X' denotes "don't care" |     |      |  |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |
| 1      | 0    | 0  | 0    |                                |     |      |  |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |
| 1      | 1    | 0  | 1    |                                |     |      |  |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |
| 1      | X    | 1  | 1    |                                |     |      |  |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |
| CFC    | 23   | active LOW open drain output. Signifies a change of configuration at the 16-frame boundary (not 8 ms in advance). Cleared after 128 ms time out (non-I <sup>2</sup> C-bus applications) or by the I <sup>2</sup> C-bus reading the status register.  |      |                                |     |      |  |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |
| SDA    | 24   | I <sup>2</sup> C-bus data input/open drain input.  |      |                                |     |      |  |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |
| SCL    | 26   | I <sup>2</sup> C-bus clock input. (Maximum speed 100 kHz).   |      |                                |     |      |  |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |
| D/S    | 27   | output pin indicating single or dual mono sound: D/S = 1 indicates dual mono; D/S = 0 indicates not dual mono. This bit is also available within the I <sup>2</sup> C-bus register map.  |      |                                |     |      |  |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |
| S/M    | 28   | output pin providing indication of the presence of mono or stereo sound. S/M = 1 indicates stereo; S/M = 0 indicates mono. This bit is also available within the I <sup>2</sup> C-bus register map.  |      |                                |     |      |  |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |

### I<sup>2</sup>C-bus FORMATS

The SAA7280 contains an I<sup>2</sup>C-bus slave transceiver permitting a master device to:-

- Read decoder status information derived from the transmitted digital audio signal
- Read an error count byte to determine the bit error rate for mute purposes
- Read additional transmitted data bits. Their purpose has yet to be defined but accessibility is provided to allow future services to be implemented in receiver software

- Write control codes to select the available analogue switching configurations
- Select the output configuration by writing control information to the device.

The device slave address is A(6:0)(R/W) = 101101X(R/W). An ADSEL pin is provided to allow selection of one of two different slave addresses via programmable address bit A0.

The SAA7280 does not acknowledge the I<sup>2</sup>C-bus general call address.

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The slave receiver format is:

$S$  SLAVE\_ADDR.0 ACK SUB\_ADDR ACK  $\overline{DATA\ BYTE\ ACK}$  P  
[.....n bytes.....]

Auto-increment of the sub-address is provided with wrap-around from 0F (HEX) to 00 (HEX).

The slave receiver data byte format, as a function of sub-address, is as follows:

The functions of these bits is as follows:

| SUB_ADDRESS | RESET VALUE | D7                  | D6    | D5               | D4  | D3   | D2    | D1    | D0    |
|-------------|-------------|---------------------|-------|------------------|-----|------|-------|-------|-------|
| 01          | 09          | M1/ $\overline{M2}$ | DMSEL | $\overline{OVS}$ | SC3 | SBEN | PORT2 | PT1EN | PORT1 |

### M1/ $\overline{M2}$

This bit selects either M1 (M1/ $\overline{M2}$  = 1) or M2 (M1/ $\overline{M2}$  = 0) when the input transmission consists of two independent mono signals (see Fig. 3).

### DMSEL

DMSEL is the dual mono selection bit. When asserted it selects M1 and M2 as the output signals if the incoming transmission consists of two independent mono signals.

The M1/ $\overline{M2}$  and DMSEL bits are exclusive-ORed with the dedicated M1/ $\overline{M2}$  and DMSEL pins respectively. By setting the

appropriate pins or bits LOW, this allows the source of these signals to be from either the I<sup>2</sup>C-bus or input pins (see Fig. 3).

### $\overline{OVS}$

Forming the active LOW over-sampling selection bit,  $\overline{OVS}$  selects between x3 over-sampled output ( $\overline{OVS}$  = 0) and non over-sampled output ( $\overline{OVS}$  = 1). The default format is for over-sampled output ( $\overline{OVS}$  = 0).

### SC3

This bit selects the polarity of the external MUTE pin.

SC3 = 1 => external MUTE is active HIGH  
SC3 = 0 => external MUTE is active LOW

Note that the external MUTE facility overrides in all modes and by default is actively LOW in the I<sup>2</sup>C-bus free mode.

### SBEN

SBEN is the sound bus enable bit. The default condition enables the sound bus (SBEN = 1).

### PORT2

PORT2 controls a bit out, providing direct access to a dedicated output pin (P2) via the I<sup>2</sup>C-bus (see Fig.3).

| DMSEL | M1/ $\overline{M2}$ | FUNCTION                          |
|-------|---------------------|-----------------------------------|
| 0     | 0                   | selects DIGITAL, L = M2<br>R = M2 |
| 0     | 1                   | selects DIGITAL, L = M1<br>R = M1 |
| 1     | 0                   | selects DIGITAL, L = M1<br>R = M2 |
| 1     | 1                   | selects DIGITAL, L = M2<br>R = M1 |

| PORT2 | PORT2 CONTROL OUTPUT STATE |
|-------|----------------------------|
| 0     | LOW                        |
| 1     | HIGH                       |

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## PT1EN

This is an actively HIGH, PORT1 enable signal. It is used to force the FLO/PORT1 pin to an input or an output.

| PT1EN | FLO/PORT1 PIN |
|-------|---------------|
| 1     | OUTPUT        |
| 0     | INPUT         |

## PORT1

PORT1 Controls a bit out, providing direct access to a dedicated output pin (PORT1) via the I<sup>2</sup>C-bus (see Fig.3).

| PORT1 | PORT1 CONTROL OUTPUT STATE |
|-------|----------------------------|
| 0     | LOW                        |
| 1     | HIGH                       |

## Slave Transmitter

The slave transmitter formats are illustrated thus:

Where S = start, A = acknowledge, P = stop.

- a) S SLAVE\_ADDR.1 A STATUS\_BYTE NA P  
In this format the bus master reads the STATUS\_BYTE once. This format is compatible with the status read from the TDA8405.
- b) S SLAVE\_ADDR.1 A STATUS\_BYTE A ERROR\_BYTE NA P  
In this format the bus master reads two bytes of STATUS\_BYTE and ERROR\_BYTE.
- c) S SLAVE\_ADDR.1 A STATUS\_BYTE A ERROR\_BYTE A AD\_BYTE\_0 A AD\_BYTE\_1 NA P  
In this format the bus master reads four bytes of STATUS\_BYTE, ERROR\_BYTE and two additional bytes, AD\_BYTE\_0 and AD\_BYTE\_1. The additional data bytes contain the eleven additional data bits AD0 to AD10 together with information regarding their status.

The bits may be defined as follows:-

### PONRES

is a power-on reset detection bit. It is set HIGH after a power-on reset or supply reduction and is cleared LOW when the STATUS\_BYTE is read.

### S/M

stereo/mono indication:

S/M = 1 indicating an incoming stereo transmission  
S/M = 0 indicating that the incoming transmission is not stereo.

### D/S

dual/single mono indication:

D/S = 1 indicating an incoming dual mono transmission  
D/S = 0 indicating that the incoming transmission is not dual mono.

### VDSP

indicates that the decoded signal is valid digital sound. When VDSP = 0 the incoming transmission carries either a 704 Kbit/s transparent data

## DATA BYTE FORMATS

| BYTE        | D7     | D6  | D5  | D4   | D3   | D2   | D1   | D0  |
|-------------|--------|-----|-----|------|------|------|------|-----|
| STATUS_BYTE | PONRES | S/M | D/S | RSSF | VDSP | OS   | LAST | CFC |
| ERROR_BYTE  | E7     | E6  | E5  | E4   | E3   | E2   | E1   | E0  |
| AD_BYTE_0   | AD7    | AD6 | AD5 | AD4  | AD3  | AD2  | AD1  | AD0 |
| AD_BYTE_1   | OVW    | SAD | 0   | CI2  | CI1  | AD10 | AD9  | AD8 |

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INDICATOR BITS FUNCTIONAL TRUTH TABLE

| TRANSMISSION                                      | C1 | C2 | C3 | S/M | D/S | VDSP | OS |
|---|----|----|----|-----|-----|------|----|
| STEREO  | 0  | 0  | 0  | 1   | 0   | 1    | 1  |
| M1 + M2   | 0  | 1  | 0  | 0   | 1   | 1    | 1  |
| M1 + DATA   | 1  | 0  | 0  | 0   | 0   | 1    | 1  |
| TRANS. DATA                                       | 1  | 1  | 0  | 0   | 0   | 0    | 1  |
| ANY CURRENTLY UNDEFINED COMBINATION OF C1, C2, C3 |    |    |    | 0   | 0   | 0    | 1  |
| DECODER UNSYNCHRONIZED ( $\overline{OS} = 0$ )    |    |    |    | 0   | 0   | 0    | 0  |

channel or a currently undefined format is being received.

### RSSF

is the reserve sound switching flag indication equal to the C4 bit in the NICAM transmission. RSSF = 1 when the FM sound signal is carrying the same programme material as the digitally modulated carrier (specifically the M1 signal in the case of a dual mono transmission). RSSF = 0 when the FM signal is not reproduced within the digital signal.

### $\overline{OS}$

provides an active LOW indication that the decoder is out of sync. If  $\overline{OS} = 1$  the decoder is frame synchronized and has obtained CO (16 frame) sync. If  $\overline{OS} = 0$ , the decoder is out of sync. and the indicator bits are as given in the truth table.

### LAST

is the logical AND of VDSP and RSSF 'OR' FLO, i.e. LAST = VDSP.(RSSF + FLO). It provides an I<sup>2</sup>C-bus indicator regarding the status of the output pin LAST.

### $\overline{CFC}$

signals a change of configuration at the 16-frame boundary. It is cleared to '1' by the I<sup>2</sup>C-bus reading the status register or after 128 ms time out for non-I<sup>2</sup>C-bus applications.

### E7-E0

is an error count byte which counts the number of error flags. The maximum count (255) is held, becomes invalid and is cleared when it is read by the I<sup>2</sup>C-bus status register.

### AD10-AD0

are the additional data bits from the transmission and are updated every 1 ms. This provides a data capacity of 11 Kbit/s.

### SAD

is the 'status additional data' bit. This is set to '1' when new bits AD10-AD0 are latched into the I<sup>2</sup>C-bus registers. It is automatically reset to '0' when AD\_BYTE\_1 is read by the bus master.

### OVW

is the overwrite indicator for the additional data. This bit is set as new additional data bits are latched into the I<sup>2</sup>C-bus registers when

SAD = 1, i.e. when the transmission overwrites additional data bits which have not been read by the bus master. This bit is automatically reset to '0' when AD\_BYTE\_1 is read by the bus master.

### C11-C12

represent the CIB bits which are extracted by a majority logic process from the parity checks of the last ten samples in a frame (samples 55 to 64). C11 will be conveyed by the parity grouping of samples 55 to 59 and C12 will be conducted by the parity grouping of samples 60 to 64. Both parity groups will be even for UK transmissions such that C12 = 0 and C11 = 0. The transmissions of countries following the specification issued by the EBU (Doc. SPB424; Digital sound transmissions in terrestrial television) will allow odd or even parity groups, thus providing an additional 2 Kbit/s data capacity.



# Terrestrial Digital Sound Decoder (TDSD)

SAA7280

## LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

| SYMBOL     | PARAMETER                        | MIN.  | MAX.         | UNIT |
|------------|----------------------------------|-------|--------------|------|
| $V_{DD}$   | supply voltage (all supplies)    | -0.3  | +6.5         | V    |
| $V_I$      | input voltage (any input)        | -0.3  | $V_{DD}+0.5$ | V    |
| $V_O$      | output voltage                   | -0.3  | $V_{DD}+0.5$ | V    |
| $V_{stat}$ | electrostatic handling *         | -2000 | +2000        | V    |
| $I_{IOK}$  | DC input or output diode current | -     | $\pm 20$     | mA   |
| $I_{Omax}$ | output current (each output)     | -     | $\pm 10$     | mA   |
| $T_{amb}$  | ambient operating temperature    | 0     | +70          | °C   |
| $T_{stg}$  | storage temperature range        | -30   | +125         | °C   |

### Note

\* Electrostatic handling ratings equivalent to discharging a pulse with a 15 ns rise time from a 100 pF capacitor through a 1.5 k $\Omega$  resistor.

## CHARACTERISTICS

 $V_{DD} = 4.5$  to  $5.5$  V;  $T_{amb} = 0$  to  $+70$  °C

| SYMBOL   | PARAMETER                | CONDITIONS      | MIN.        | TYP. | MAX.          | UNIT |
|--|--------------------------|-----------------|-------------|------|---------------|------|
| <b>Supply</b>  |                          |                 |             |      |               |      |
| $V_{DD}$   | supply voltage           | $V_{SS} = 0$ V  | 4.5         | 5    | 5.5           | V    |
| <b>Inputs <math>\overline{RESET}</math></b>  |                          |                 |             |      |               |      |
| $V_{T+}$   | positive going threshold | Schmitt trigger | 2.2         | -    | -             | V    |
| $V_{T-}$   | negative going threshold | Schmitt trigger | -           | -    | 0.8           | V    |
| <b>TEST, ADSEL, DATA, <math>\overline{MUTE}</math>, DMSEL, M1/M2 and FLO/PORT1</b> |                          |                 |             |      |               |      |
| $V_{IH}$   | input voltage HIGH       |                 | 2           | -    | $V_{DD}+0.5V$ | V    |
| $V_{IL}$   | input voltage LOW        |                 | 0           | -    | 0.8           | V    |
| $C_I$  | input capacitance        |                 | -           | -    | 10            | pF   |
| <b>SDA and SCL</b>   |                          |                 |             |      |               |      |
| $V_{IH}$   | input voltage HIGH       |                 | $0.7V_{DD}$ | -    | $V_{DD}+0.5V$ | V    |
| $V_{IL}$   | input voltage LOW        |                 | 0           | -    | $0.3V_{DD}$   | V    |
| $C_I$  | input capacitance        |                 | -           | -    | 10            | pF   |
| <b>XIN and XOUT (crystal oscillator)</b>   |                          |                 |             |      |               |      |
| gm   | transconductance         |                 | -           | -    | 12            | mA/V |
| $A_v$  | small signal gain        | at 25 MHz       | -           | 7.2  | -             | -    |
| $C_I$  | input capacitance        |                 | -           | 10   | -             | pF   |
| $C_{FB}$   | feedback capacitance     |                 | -           | 5    | -             | pF   |
| $C_O$  | output capacitance       |                 | -           | 10   | -             | pF   |

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| SYMBOL   | PARAMETER                   | CONDITIONS            | MIN.   | TYP.   | MAX.   | UNIT          |
|--|-----------------------------|-----------------------|--------|--------|--------|---------------|
| <b>Outputs SDAT, STIM, SCLK, PCLK and EDET</b>     |                             |                       |        |        |        |               |
| $V_{OH}$   | output voltage HIGH         | $I_o = -2 \text{ mA}$ | 2.4    | -      | -      | V             |
| $V_{OL}$   | output voltage LOW          | $I_o = 2 \text{ mA}$  | -      | -      | 0.4    | V             |
| $C_L$  | load capacitance            |                       | -      | -      | 50     | pF            |
| <b>S/M, D/S, LAST, PORT2 and FLO/PORT1</b>         |                             |                       |        |        |        |               |
| $V_{OH}$   | output voltage HIGH         | $I_o = -4 \text{ mA}$ | 2.4    | -      | -      | V             |
| $V_{OL}$   | output voltage LOW          | $I_o = 4 \text{ mA}$  | -      | -      | 0.4    | V             |
| $C_L$  | load capacitance            |                       | -      | -      | 50     | pF            |
| <b>CFC</b>   |                             |                       |        |        |        |               |
| $V_{OL}$   | output voltage LOW          | $I_o = 4 \text{ mA}$  | -      | -      | 0.4    | V             |
| $C_L$  | load capacitance            |                       | -      | -      | 50     | pF            |
| <b>SDA</b>   |                             |                       |        |        |        |               |
| $V_{OL}$   | output voltage LOW          | $I_o = 4 \text{ mA}$  | -      | -      | 0.4    | V             |
| $C_L$  | load capacitance            |                       | -      | -      | 400    | pF            |
| <b>Timing</b>                                      |                             |                       |        |        |        |               |
| $f_{XTAL}$   | crystal operating frequency |                       | 15.725 | 17.472 | 19.219 | MHz           |
| <b>Timing of inputs: data with respect to PCLK</b> |                             |                       |        |        |        |               |
| $t_{SU}$   | set-up time                 |                       | 100    | -      | -      | ns            |
| $t_{HD}$   | hold time                   |                       | 100    | -      | -      | ns            |
| <b>SDA and SCL (see Fig. 5)</b>                    |                             |                       |        |        |        |               |
| $f_{SCL}$  | operating frequency         |                       | 1      | -      | 100    | kHz           |
| $t_r$  | input rise time             |                       | -      | -      | 1      | $\mu\text{s}$ |
| $t_f$  | input fall time             |                       | -      | -      | 300    | ns            |
| $t_{BUF}$  | bus free time               |                       | 4      | -      | -      | $\mu\text{s}$ |
| $t_{LOW}$  | SCL LOW time                |                       | 4      | -      | -      | $\mu\text{s}$ |
| $t_{HIGH}$   | SCL HIGH time               |                       | 4      | -      | -      | $\mu\text{s}$ |
| $t_{SU:STA}$                                       | start code set-up time      |                       | 4      | -      | -      | $\mu\text{s}$ |
| $t_{HD:STA}$                                       | start code hold time        |                       | 4      | -      | -      | $\mu\text{s}$ |
| $t_{SU:DAT}$                                       | data set-up time            |                       | 250    | -      | -      | ns            |
| $t_{HD:DAT}$                                       | data hold time              |                       | 0      | -      | -      | ns            |
| $t_{SU:STO}$                                       | stop code set-up time       |                       | 4      | -      | -      | $\mu\text{s}$ |
| $t_{CYC}$  | SCL cycle time              |                       | 10     | -      | -      | $\mu\text{s}$ |
| <b>Timing of outputs: SDA</b>                      |                             |                       |        |        |        |               |
| $t_{OH}$   | hold time                   |                       | 250    | -      | -      | ns            |
| $t_{OD}$   | delay time                  |                       | -      | -      | 3      | ns            |
| <b>SDAT, STIM and SCLK</b>                         |                             |                       |        |        |        |               |
| $t_r/t_f$  | rise/fall time              |                       | -      | -      | 20     | ns            |

# Terrestrial Digital Sound Decoder (TDSD)

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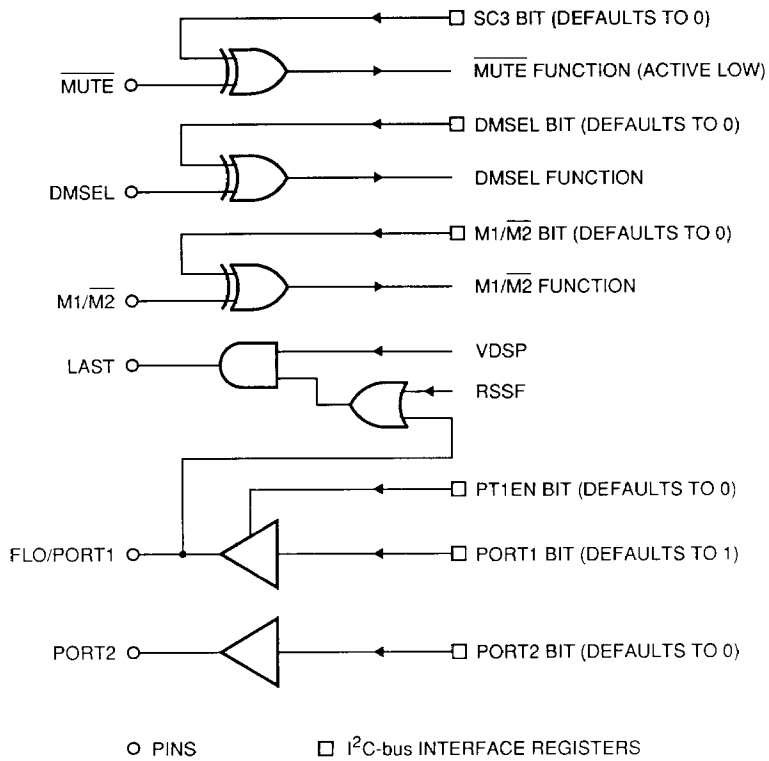
| SYMBOL   | PARAMETER       | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|-----------------|------------|------|------|------|------|
| <b>SCLK I<sup>2</sup>S over-sampled output (see Figs. 6 and 7)</b> |                 |            |      |      |      |      |
| t <sub>CK</sub>  | clock period    |            | -    | 343  | -    | ns   |
| t <sub>CKH</sub>   | clock HIGH time |            | -    | 172  | -    | ns   |
| t <sub>CKL</sub>   | clock LOW time  |            | -    | 172  | -    | ns   |
| <b>SCLK I<sup>2</sup>S non over-sampled output</b>                 |                 |            |      |      |      |      |
| t <sub>CK</sub>  | clock period    | see note 1 | 1.03 | -    | 1.2  | μs   |
| t <sub>CKH</sub>   | clock HIGH time |            | -    | 515  | -    | ns   |
| t <sub>CKL</sub>   | clock LOW time  |            | 515  | -    | 687  | ns   |
| <b>SDAT, STIM with respect to SCLK (see Fig. 7)</b>                |                 |            |      |      |      |      |
| t <sub>SU</sub>  | set-up time     |            | 40   | -    | -    | ns   |
| t <sub>HD</sub>  | hold time       |            | 5    | -    | -    | ns   |
| <b>PCLK</b>  |                 |            |      |      |      |      |
| t <sub>CK</sub>  | clock period    |            | 1.3  | 1.37 | -    | μs   |
| t <sub>CKH</sub>   | clock HIGH time |            | 650  | 687  | -    | ns   |
| t <sub>CKL</sub>   | clock LOW time  |            | 650  | 687  | -    | ns   |
| t <sub>r</sub> /t <sub>f</sub>                                     | rise/fall time  |            | -    | -    | 20   | ns   |

**Note**

The clock period for SCLK in I<sup>2</sup>S non over-sampled mode alternates between 1.03 μs and 1.2 μs.

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(TDSD)

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Fig.3 Conceptual diagram of SAA7280 control functions and ports.

# Terrestrial Digital Sound Decoder (TDSD)

SAA7280

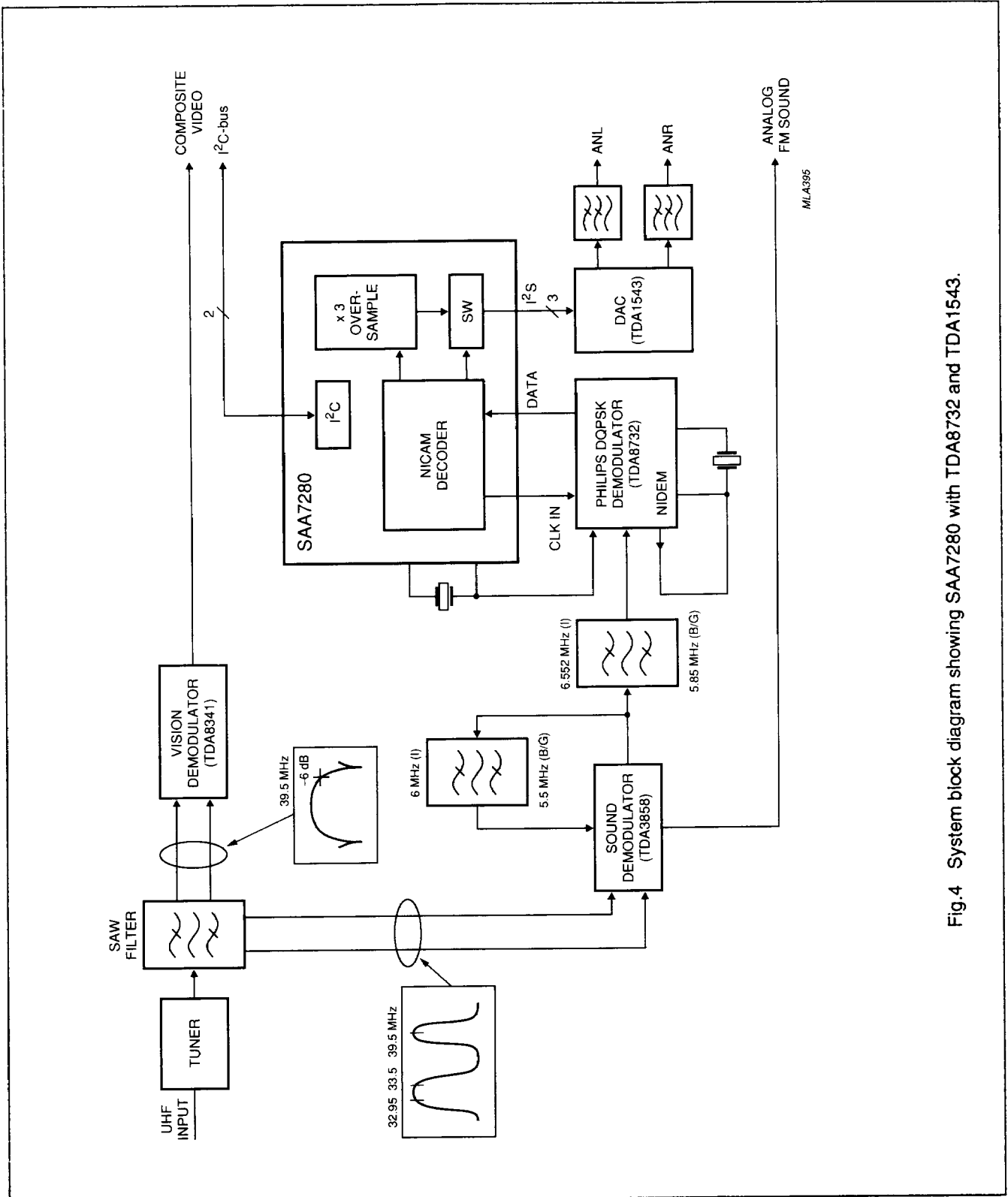


Fig.4 System block diagram showing SAA7280 with TDA8732 and TDA1543.

Terrestrial Digital Sound Decoder  
(TDSD)

SAA7280

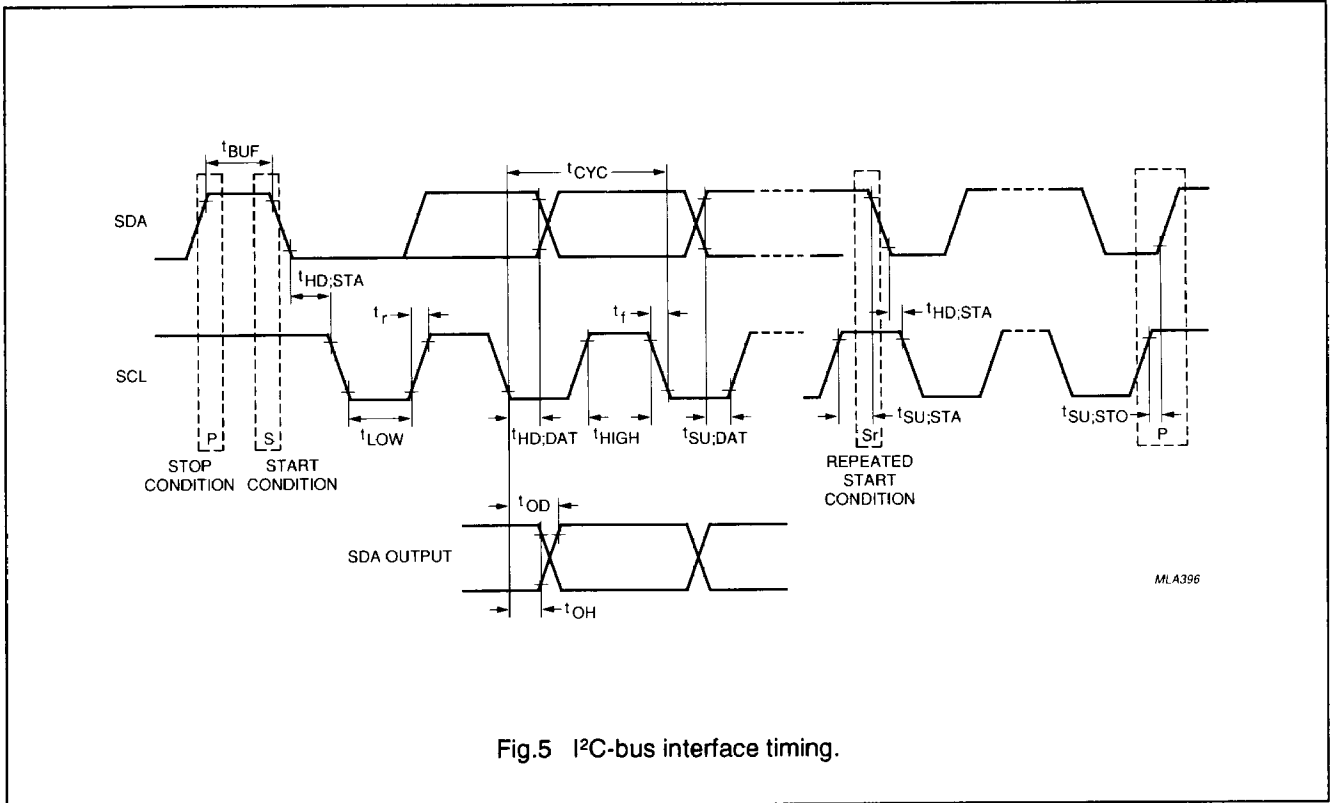
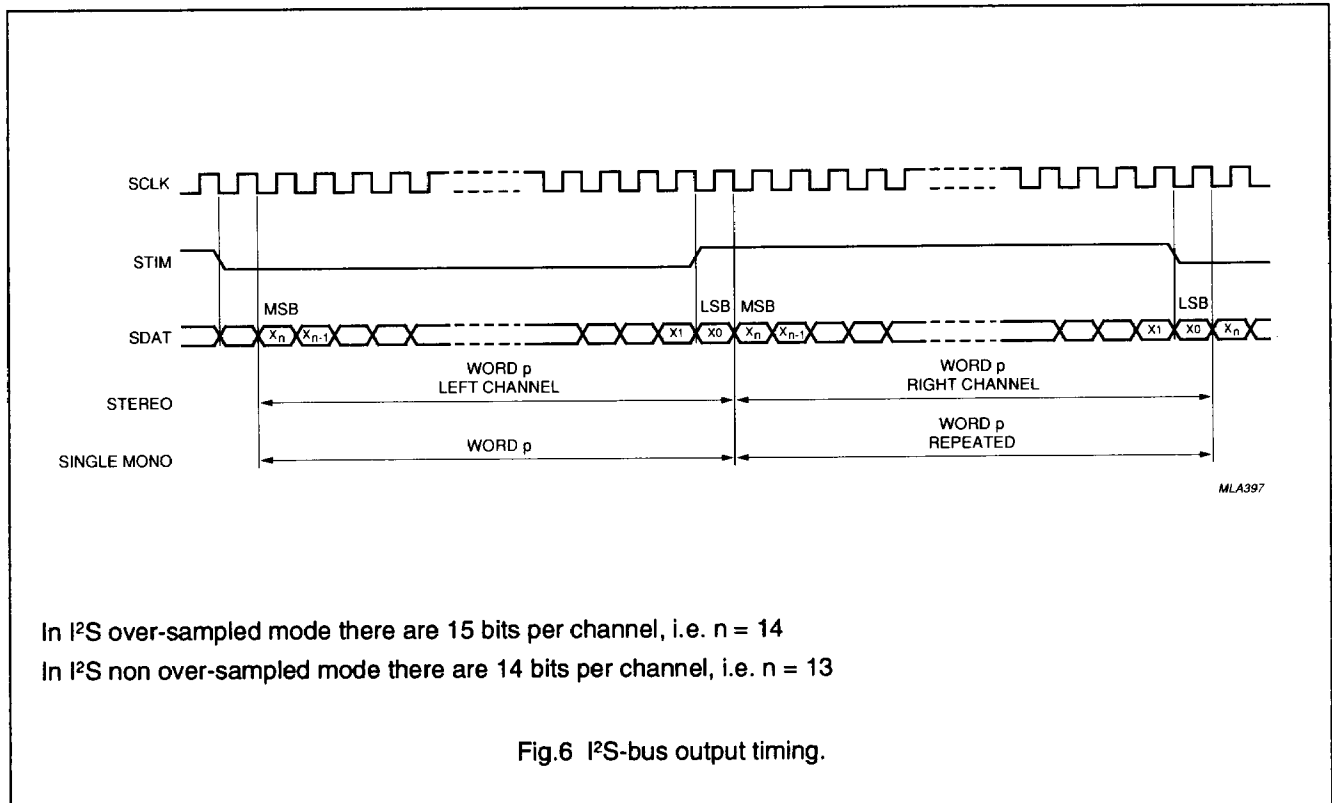


Fig.5 I<sup>2</sup>C-bus interface timing.

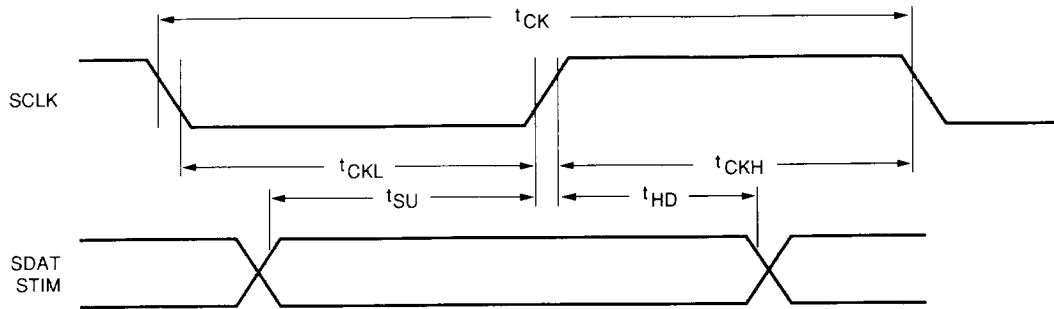


In I<sup>2</sup>S over-sampled mode there are 15 bits per channel, i.e.  $n = 14$   
 In I<sup>2</sup>S non over-sampled mode there are 14 bits per channel, i.e.  $n = 13$

Fig.6 I<sup>2</sup>S-bus output timing.

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(TDSD)

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Fig.7 Data output timing.

# Terrestrial Digital Sound Decoder (TDSD)

## SAA7280

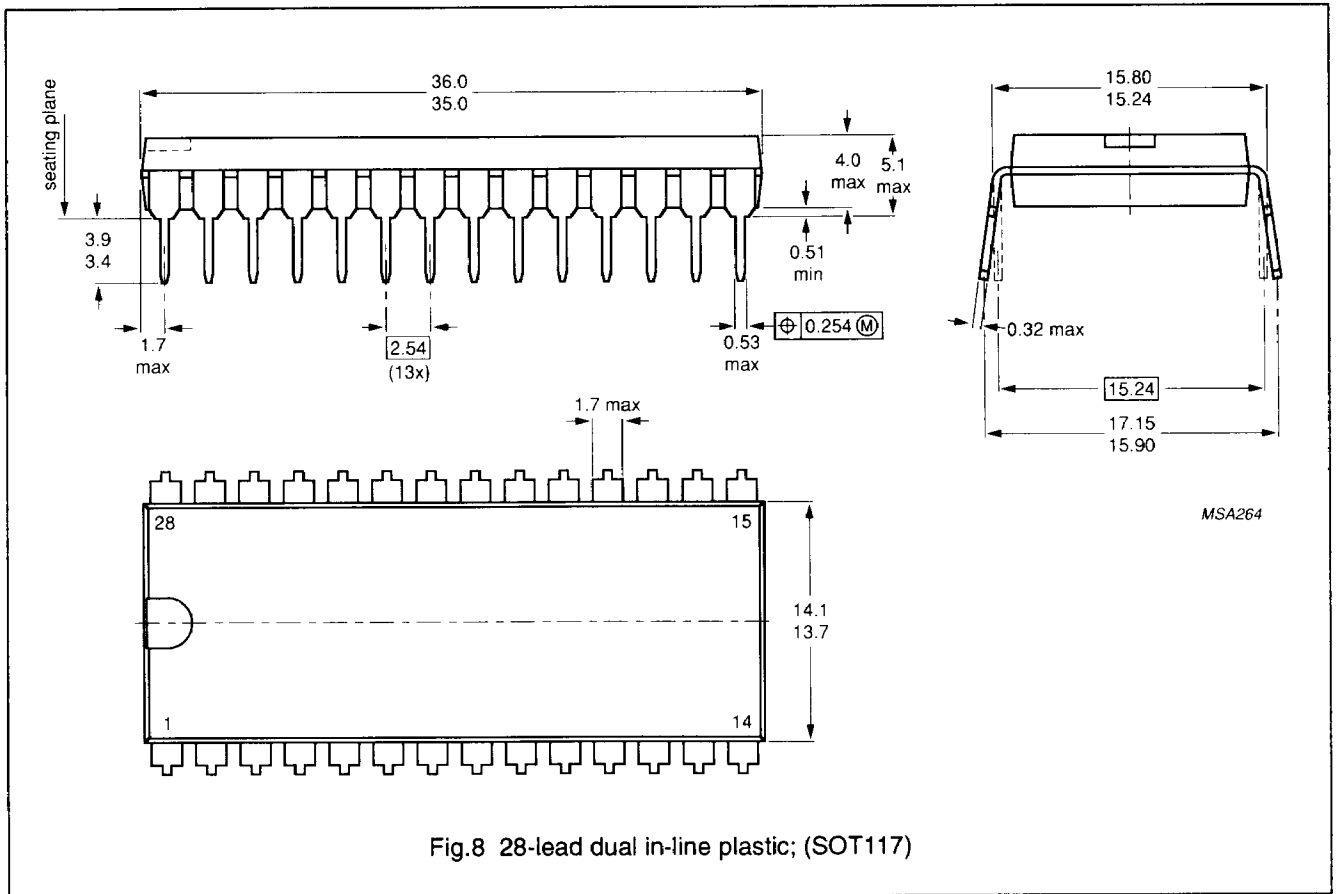


Fig.8 28-lead dual in-line plastic; (SOT117)



# Terrestrial Digital Sound Decoder (TDSD)

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## SOLDERING

### Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

### REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

## DEFINITIONS

| <b>Data sheet status</b>   |   |
|--|---|
| Objective specification  | This data sheet contains target or goal specifications for product development        |
| Preliminary specification  | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification  | This data sheet contains final product specifications.                                |
| <b>Application information</b>   |   |
| Where application information is given, it is advisory and does not form part of the specification.  |   |
| <b>Limiting values</b>   |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |

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